NCHRP 35-02
Synthesis
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Chip Seal Best Practices
What is a Best Practice?

For the purpose of this synthesis, a best practice is defined as:

“Any successful practice identified in the literature review and confirmed in the survey responses”
Lit Review & Survey

- Over 120 publications representing 80 years of chip seal research
- A total of 92 individual responses from:
  - 42 US states, 12 US cities and counties,
  - 10 Canadian provinces, 1 territory, and 2 cities,
  - 4 Australian states,
  - 2 New Zealand states,
  - 2 public agencies in the United Kingdom, and
  - 1 agency in South Africa
Chip Seal Service Life

Typical Chip Seal Service Life (Years)

- United States: 5.76 years
- Canada: 5.33 years
- AU, NZ, UK, SA: 9.60 years
Warranties

Warranty Requirements

- United States: 19% Yes, 81% No
- Canada: 11% Yes, 89% No
- AU, NZ, UK, SA: 100% Yes

Legend: ■ Yes  □ No
Best Practices Identified

- 38 Best Practices identified in:
  - Design and Material Selection.
  - Contract Administration, Warranties, and Performance Measures.
  - Construction.
  - Chip Seal Equipment and Quality Assurance/Quality Control
Best Practices in Design, and Material Selection

- Chip seal should be a PM tool applied on a regular cycle.

- Characterize the underlying road’s texture and surface hardness and use as a basis for developing the subsequent *FORMAL* chip seal design.

- Use the “Racked-in Seal” as the corrective measure for bleeding instead of the North American practice of spread fine aggregate on the bleeding surface.
Best Practices in Contract Administration, Warranties, and Performance Measures

- Let chip seal contracts in time to permit early season construction.

- Package chip seal contracts in jobs large enough to attract the most qualified contractors.

- In-house maintenance forces should be used to install chips seals in areas where the greatest care must be taken to achieve a successful product.
Best Practices in Construction

* All types chip seals should be applied in the warmest, driest weather possible.

* Patches should be completed at least 6 months prior and crack seals should be applied at least 3 months prior to the application of chip seals.

* Variable nozzles or the Australian practice of pre-spraying should be used to combat flooding in the wheel paths, a defect that makes chip seals prone to bleeding.
Best Practices in Construction

- Rolling specifications for:
  - Roller coverage, rolling patterns, and minimum rolling time.
  - Minimum rolling guidelines should generally be in the range of 3000 to 5000 square yards per hour of rolling time.

- Rolling must follow as close as practical behind the chip spreader

- Traffic control should be maintained for as long as possible to give the fresh seal the maximum amount of curing time.
Best Practices in Chip Seal Equipment and QA/QC

- Requiring chip seal contractors to use state-of-the-art computerized equipment and to control the rolling operation enhances chip seal success.

- An aggressive QC testing program combined with close inspection by experienced personnel leads to chip seal success.
Synthesis 342 Chip Seal Performance Responses
Performance Correlation Categories

- Pre-seal surface preparation.
- Ambient air and pavement temperature specifications in which chip seals can be installed
- Applying binder and aggregate
- Rolling and brooming
- Traffic control
- Post-seal measures
Pre-seal surface preparation

<table>
<thead>
<tr>
<th>Pre-seal Procedure</th>
<th>Excellent</th>
<th>Good</th>
<th>Fair</th>
<th>Poor</th>
<th>Excellent</th>
<th>Good</th>
<th>Fair</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip seal on paved asphalt surface</td>
<td>2</td>
<td>5</td>
<td>2</td>
<td>0</td>
<td>6.7%</td>
<td>11.1%</td>
<td>15.4%</td>
</tr>
<tr>
<td>Crack sealing</td>
<td>16</td>
<td>20</td>
<td>8</td>
<td>0</td>
<td>53.3%</td>
<td>44.4%</td>
<td>61.5%</td>
</tr>
<tr>
<td>Fog coat</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.0%</td>
<td>0.0%</td>
<td>0.0%</td>
</tr>
<tr>
<td>Patching</td>
<td>7</td>
<td>15</td>
<td>3</td>
<td>1</td>
<td>23.3%</td>
<td>33.3%</td>
<td>23.1%</td>
</tr>
<tr>
<td>Geotextile to retard reflective cracking</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>3.3%</td>
<td>2.2%</td>
<td>0.0%</td>
</tr>
</tbody>
</table>

Number of responses
Percentage within category

Emphasis on crack sealing enhances chip seal performance.
## Average Temperature Specifications

<table>
<thead>
<tr>
<th>Category</th>
<th>Average Ambient Air Temperature</th>
<th>Average Pavement Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Excellent</td>
<td>Good</td>
</tr>
<tr>
<td>Degrees F</td>
<td>57.9</td>
<td>57.9</td>
</tr>
<tr>
<td>No specification</td>
<td>3</td>
<td>12</td>
</tr>
<tr>
<td>Range</td>
<td>40-70</td>
<td>45-70</td>
</tr>
</tbody>
</table>

Increasing temperature specifications enhances chip seal performance.
Distributor and chip spreader specifications

<table>
<thead>
<tr>
<th>Require computerized controls on binder distributors</th>
<th>Require computerized controls on chip spreaders</th>
</tr>
</thead>
<tbody>
<tr>
<td>Excellent</td>
<td>Good</td>
</tr>
<tr>
<td>Yes</td>
<td>17</td>
</tr>
<tr>
<td>No</td>
<td>5</td>
</tr>
<tr>
<td>Yes</td>
<td>1</td>
</tr>
<tr>
<td>No</td>
<td>0</td>
</tr>
</tbody>
</table>

Requiring state-of-the-art application equipment enhances chip seal performance.
## Roller specifications

<table>
<thead>
<tr>
<th>Roller controls</th>
<th>Number of responses</th>
<th>Percentage of category population</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Excellent</td>
<td>Good</td>
</tr>
<tr>
<td>Number of passes</td>
<td>12</td>
<td>26</td>
</tr>
<tr>
<td>Rolling patterns</td>
<td>10</td>
<td>13</td>
</tr>
<tr>
<td>Speed limits</td>
<td>11</td>
<td>15</td>
</tr>
<tr>
<td>Roller weight</td>
<td>8</td>
<td>16</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Typical number pneumatic-tired rollers required</th>
<th>Number of responses</th>
<th>Percentage of category population</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Excellent</td>
<td>Good</td>
</tr>
<tr>
<td>One</td>
<td>4</td>
<td>9</td>
</tr>
<tr>
<td>Two</td>
<td>12</td>
<td>21</td>
</tr>
<tr>
<td>Three</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>Four</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Emphasis on rolling enhances chip seal performance
## Brooming controls

The table below shows the average time span between final rolling and initial brooming for different categories.

<table>
<thead>
<tr>
<th>Category</th>
<th>Excellent</th>
<th>Good</th>
<th>Fair</th>
<th>Poor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hours</td>
<td>5.5</td>
<td>15.9</td>
<td>31.5</td>
<td>0</td>
</tr>
</tbody>
</table>

Requiring brooming as soon as feasible enhances chip seal performance.
## Traffic Control Period

<table>
<thead>
<tr>
<th>Category</th>
<th>Typical maximum reduced speed limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPH</td>
<td>Excellent</td>
</tr>
<tr>
<td></td>
<td>31.4</td>
</tr>
</tbody>
</table>

| Time span between final rolling and opening to *reduced speed* traffic |
|---------------------------|-----------------|
| Minutes                  | 48.2            | 68.1    | 43.2    | 60.0 |

| Average time span between final rolling and opening to *full speed* traffic |
|-------------------------------|-----------------|
| Hours                         | 28.0            | 19.8    | 18.5    | 8.0  |

Maintaining traffic control as long as possible enhances chip seal performance.
### Traffic Control Methods

<table>
<thead>
<tr>
<th>Required traffic control measures</th>
<th>Number of responses</th>
<th>Percentage of category population</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Excellent</td>
<td>Good</td>
</tr>
<tr>
<td>Reduced speed</td>
<td>18</td>
<td>27</td>
</tr>
<tr>
<td>Interim pavement markings &amp; devices</td>
<td>14</td>
<td>22</td>
</tr>
<tr>
<td>Pilot vehicles</td>
<td>16</td>
<td>24</td>
</tr>
<tr>
<td>Flaggers</td>
<td>20</td>
<td>25</td>
</tr>
</tbody>
</table>

Increased use traffic control measures enhances chip seal performance.
Traffic Control Measures

- Traffic control measures keep traffic where:
  - It will do the most good
  - Or do the least harm
- New Zealand spec requires the cones to be moved every 3-4 hours to shift the traffic across the entire sealed surface
- Considered “final rolling” in TNZ spec
- Personal work in NZ shows excellent chip seals where policy requires ADT > 25K to justify HMAC surface
New Zealand has continued to invest in chip seal research.

Hot-mix asphalt only used in areas with ADT >25,000

NZ uses a rational design method (TNZP17) based on engineering inputs:

- Aggregate angularity, aggregate absorption,
- Traffic volume, road geometry
- Average least dimension (ALD) of aggregate,
- Pavement absorption and texture depth,
Chip Seal Performance

Typical Chip Seal Service Life

Years

United States  Canada  New Zealand

0  2  4  6  8

DOTD
Typical “Sealed” Road in New Zealand
Water Retexturizing

- New Zealand Contractor has a patented ultra-high pressure watercutter for removing excess bitumen from the road and restoring the microtexture of polished aggregates and chips in road surfacings.
Watercutter Retexturizing in New Zealand

BEFORE

AFTER
New Zealand Performance-based Chip Seal Design

- TNZP17 minimum binder application rate is determined by:
  - Percentage of voids to be filled,
  - Total available voids, and
  - Desired thickness of the seal

- Adjustments for aggregate and traffic levels are added to derive a design voids factor.

- Design voids factor is multiplied by the ALD of the aggregate to get the basic binder application rate
New Zealand Performance-based Chip Seal Design

- Adjustments then made for:
  - Underlying pavement condition:
    - Hardness, existing texture, oxidation
  - Geometric factors:
    - narrow lanes, climbing lanes, and turning locations. traffic is channeled into confined wheel paths such as on single lane bridges, tight radius curves or pavements with confined lane widths,

- Some of the allowances may be negative -> design binder application rate may be lower than the base binder application rate.
New Zealand Performance Criteria

\[ Td_1 = 0.07 \text{ ALD} \log Y_d + 0.9 \]

Where: \( Td_1 \) = texture depth in one year (mm)

\( Y_d \) = design life in years

\( \text{ALD} \) = average least dimension of the aggregate
Experimental Set-up

Current TNZP17 Sand Circle Test

Digital Imaging to Replace TNZP17 Sand Circle Test
Satisfactory texture; Grade 3 Single Chip; SC = 175 mm

Very heavy flushing; Grade 3 Single Chip; SC=300mm
Current Status

- Factorial analysis looking for combinations of ring output that furnishes the best correlation is encouraging.
Final Word

The Chip Seal Rule of Thumb:

“Place the right treatment, on the right road, at the right time”

(Galehouse, Moulthrop, & Hicks, 2003)
Questions / Comments

Thank You for Your Time